LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A system comprising:

a sample network that provides plural samples of an input signal state for different time instances of the input signal, each of the plural samples corresponding to the input signal delayed by a known amount of time;

a detector that determines the frequency of the input signal based on (i) samples of the input signal state received by the detector for different time instances of the input signal residing within less than or equal to one period of the input signal, and (ii) the known amount of time for each of the plural samples, the detector provides a value that represents the determined frequency of the input signal;

a comparator that provides a comparator signal based on a comparison of the value of the frequency for the input signal and a value of a desired frequency; and

a controller operative to implement adjustments to a clock signal based on the comparator signal.

2. (Previously Presented) The system of claim 1, the sample network further comprising a plurality of storage elements arranged to provide output samples corresponding to the plural samples of the input signal state.

3. (Previously Presented) The system of claim 2, further comprising delay elements associated with at least a substantial number of the storage elements, the delay elements providing respective delayed clock signals to clock the at least a substantial number of the storage elements to sample the input signal at different time intervals and thereby provide the plural samples of the input signal state.

4. (Previously Presented) The system of claim 3, wherein the input signal is delayed by the delay elements to provide the respective delayed clock signals.

5. (Previously Presented) The system of claim 2, further comprising an oscillator that provides a clock signal for activating at least a substantial number of the storage elements to provide the plural samples of the input signal state to the detector.

6. (Original) The system of claim 5, wherein the oscillator provides the clock signal at a frequency that is one of lower and higher than the frequency of the input signal.

7. (Previously Presented) The system of claim 5, further comprising delay elements associated with at least N of the storage elements, where N+1 is a positive integer denoting the number of the storage elements, the delay elements each having a fixed known amount of delay for providing respective clock edges for clocking the at least N of the storage elements, each of the respective clock edges corresponding to a different delayed version of the clock signal such that a different time instance of the input signal is latched into each of the at least N of the storage elements.

8. (Original) The system of claim 7, wherein the delay elements are connected in series so that the amount of delay for a given clock edge corresponds to an aggregate amount of delay according to the number of delay elements in the path from the oscillator to the storage element activated by the given clock edge.

9. (Previously Presented) The system of claim 2, wherein an output of a preceding storage element is coupled to an input of a next storage element.

10. (Previously Presented) The system of claim 8, wherein the input signal is provided directly to an input of each of the storage elements such that the storage elements provide the output samples based on delayed activation by each given clock edge.

11. (Previously Presented) The system of claim 1, wherein the sample network further comprises a plurality of storage elements activated at time intervals to latch output samples concurrently to the detector corresponding to the samples of the input signal state.

12. (Canceled)

13. (Previously Presented) The system of claim 1, further comprising an oscillator that generates the input signal as a clock signal having a frequency based on a controller output signal provided by the controller.

14. (Original) An integrated circuit chip comprising the system of claim 1.

15. (Currently Amended) A system comprising:

a plurality of storage elements, the plurality of storage elements being clocked to latch different time instances of an input signal to provide corresponding output samples of the input signal sufficient for determining a frequency value of the input signal;

a plurality of delay elements associated with at least a substantial number of the storage elements, each of the delay elements delaying a sample signal by a respective known amount of time to provide a respective clock signal corresponding to a delayed version of the sample signal that clocks a respective one of the at least a substantial number of the storage elements to latch a respective one of the different time instances of the input signal to provide at least a portion of the corresponding output samples; and

a detector that provides a frequency value for the input signal based (i) on output samples that correspond to different time instances of the input signal and (ii) the known amount of time for each respective delay element;

wherein the input signal comprises the sample signal, the input signal being delayed by the plurality of delay elements to provide the respective delayed clock signals for clocking the at least a substantial number of the storage elements to latch the different time instances of the input signal into the storage elements.

16-17. (Canceled)

18. (Cancelled)

19. (Canceled)

20. (Previously Presented) The system of claim 15, further comprising an oscillator that provides the sample signal to at least one of the plurality of delay elements based on which the

respective clock signals are provided for latching the different time instances of the input signal into the plurality of storage elements to provide the corresponding output samples.

21. (Previously Presented) The system of claim 20, wherein each of the respective clock signals corresponds to a different delayed version of the sample signal.

22. (Previously Presented) The system of claim 21, wherein the delay elements are connected in series so that the amount of delay for a given clock signal corresponds to an aggregate amount of delay according to the number of delay elements in the path from the oscillator to the storage element activated by the given clock signal.

23. (Previously Presented) The system of claim 22, wherein the input signal is provided directly to an input of each of the storage elements such that the storage elements provide the corresponding output samples based on when each of the storage elements are clocked by the respective clock signals.

24. (Previously Presented) The system of claim 15, wherein the plurality of storage elements are clocked by the respective clock signals at predetermined time intervals to latch the output samples to the detector concurrently to provide the corresponding output samples that represent different time instances of signal state for the input signal.

25. (Previously Presented) A frequency detection system comprising:

means for sampling an input signal having an unknown frequency and for providing plural indications of signal state associated with different time instances of the input signal delayed for different known amounts of time; and

means for determining a frequency for the input signal based on (i) the plural indications of signal state received by the means for determining, that correspond to time instances of the input signal residing within a single period of the input signal, and (ii) the known amounts of time;

means for providing a corresponding frequency value for the determined frequency;

means for comparing the frequency value relative to a desired frequency value; and

means for controlling the frequency of the input signal based on the comparison of the frequency of the input signal and the desired frequency.

26. (Original) The system of claim 25, further comprising means for delaying sampling of the input signal by selected parts of the means for sampling.

27. (Original) The system of claim 25, wherein the means for delaying further comprises means for delaying a clock signal to provide activation signals that control sampling performed by the means for sampling.

28. (Original) The system of claim 25, wherein the means for sampling further comprising a plurality of means for storing signal state information based on an activation signal.

29. (Canceled)

30. (Previously Presented) A method comprising:

sampling a signal at predetermined and spaced apart time intervals to provide a plurality of output samples indicative of signal state for different time instances of the signal;

determining a frequency value for the signal that represents a frequency of the signal based on (i) the output samples received at a detector that correspond to time instances of the signal residing within a single period of the signal, and (ii) the predetermined and spaced apart time intervals;

controlling an oscillator to provide the signal at a frequency based on a comparison of the frequency value for the signal relative to a desired frequency value.

31. (Original) The method of claim 30, the sampling further comprising activating a plurality of storage elements to provide the plurality of output samples concurrently.

32. (Previously Presented) The method of claim 31, the activation further comprising generating clock edges at the predetermined and spaced apart time intervals that are provided to activate the plurality of storage elements.

33. (Original) The method of claim 32, the generation of clock edges further comprising delaying a clock signal to provide the clock edges.

34. (Previously Presented) The method of claim 31, further comprising delaying propagation of the signal through the plurality of storage elements having known amounts of delay to establish the predetermined and spaced apart time intervals at which the signal is sampled.

35. (Original) The method of claim 31 further comprising providing a clock signal to control the activation of the storage elements.

36. (Canceled)

37. (Previously Presented) The method of claim 30, wherein the controlling further comprises providing at least one control signal to cause the oscillator to one of increase, decrease and not change the frequency of the signal.

38. (Previously Presented) The system of claim 15 wherein the frequency value is expressed in units of an inverse of a period of the input signal.